DESIGN OF 7T SRAM FOR SECURITY ORIENTED APPLICATIONS

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Abstract:

Memory is a crucial component of any modern integrated device because of the ubiquity of digital data. Additionally, it contributes significantly to the overall circuit power. The semiconductor industry is increasingly focused on nanotechnology as the need for portable devices rises. However, static random access memory is a major contributor to battery consumption in portable devices. Since technology is shrinking,When compared to the fluctuating power needs, leakage power plays a significant influence. Therefore, in order to meet the current requirement for reduced power usage, we included a power gating approach into our proposed SRAM memory. In addition, we included an additional Function to cut down on leaking power. Since NMOS devices have a higher leakage current compared to PMOS devices of the same feature size. Pass transistors in SRAM cells are switched from NMOS to PMOS to further decrease leakage power consumption.

Keywords: RAM, SRAM, PMOS,NMOS.

INTRODUCTION

Memory architectures are now an integral feature of all VLSI designs. Memory chips made of semiconductors may function independently, but they also play a crucial role in very large scale integration (VLSI) systems. The semiconductor memory's core storage components haven't evolved much in a long time. Despite the passage of time, various types of storage cells may be Overall, these cells provide the optimal compromise between many design considerations, including economy of arrangement, performance, size, and sensitivity to noise. MOS random access memory (RAMs) are the focus of this chapter, namely their read and write operations. DRAMs and SRAMs are the two main categories into which traditional RAMs fall. In the former case, the cell state is commonly kept as charge on a capacitor inside a single-transistor storage device. No storage capacitors are perfect, hence it's necessary to recharge them at regular intervals, hence the word "dynamic." Static RAMs, on the other hand, store the cell state as a voltage differential using a bistable device like an inverter loop. As long as energy is being delivered, the status of these components will be maintained. When compared to a DRAM cell, the simplest SRAM cell is far more involved and takes up more space.SRAM and DRAM are often used in system architecture for a variety of reasons.There are several factors to consider while designing, such as density, speed, volatility, cost, and more. Before choosing memory for a 2 system, several issues need to be taken into account. The static random-access memory (SRAM) design is the focus of this study. SRAM, or static random access memory, is a kind of random access memory that stores information in a static format for as long as the power is on. The basic components of a static random access memory (SRAM) are two cross-coupled inverters that may hold the stable states 0 or 1, and two access transistors that are utilized during reading and writing. There are six metal oxide semiconductor field effect transistors (MOSFET) needed to store a single memory bit. An SRAM may function in one of three distinct modes. The three modes are HOLD, READ, and WRITE. By holding the word line low, we can prevent the access transistor from connecting to the data lines. As long as both inverters are linked to the power source, they will continue to reinforce each other. The process is currently in the HOLD state. In contrast, the world line is set high in READ and WRITE modes to provide cross-coupled inverters access to the bit lines. Before beginning the read cycle, both bit lines are charged to a high voltage. When a high value is asserted on the word line WL, the inverter stores a zero, and the voltage on one of the bit lines drops ever-so-slightly as a result. The data is either a 0 or a 1 depending on the voltage level, which is read by a sensing amplifier. The first step of the write cycle is to apply the write voltage to the bit lines. Bit line bar must be set to 0 and bit line must be set to 1 in order to write a 1 into the SRAM cell. A high

voltage is claimed for WL, along with the value to be stored in the cell. On-site static random access memory (SRAM) utilization is on the rise as the semiconductor industry expands rapidly. Depending on its intended use, different SRAM design factors will need to be optimized. In contrast to the recent artificial neural networks (ANNs) applications, graphics (GPU) processors, servers, and other high end applications, where energy is traded off to achieve high performance, applications like the Internet of Things (IoTs), body sensor nodes (BSNs), wearable electronics, and image processing require robustness and energy efficiency1.2 Furthermore, research has been made possible by the ability to identify and respond to the mobile and ambient environment (such as voice, occupancy, and mobility) from the wireless IoT sensor data in the case of wearable IoT apps (like Google Glass, Fitbit, and Pebble). SRAM has been the repeated design of this data storage and comprises the majority of the system size, allowing for all of these sensors to gather and evaluate the run time data by temporarily storing it in a memory.3 As a result, SRAM's impact on the system's total power consumption cannot be overstated. Short channel effects, data storage stability, and leakage currents are only some of the problems that occur when CMOS technology becomes smaller. Since our nano-CMOS technology employs such a low threshold voltage, sub threshold leakage is the primary leakage contributor. Leakage current intensity is affected by numerous variables, including supply voltage, temperature, dimensions, and process parameters such (threshold voltage). In addition to leakage currents from hot-carrier injection and gate oxide tunnelling, there are additional sources, such as reverse bias, junction leakage, gate-induced drain leakage, and gate-induced current.

CURRENT APPROACH:

Smart cards and mobile phones, for example, rely heavily on cryptographic devices that can store private data due to their widespread use over the last several decades. Known as SCA, side channel analysis is a hazard to these gadgets since it uses details about their physical actions to steal private information. Due to their effectiveness and the ease with which they may be implemented, PA assaults are often cited as examples of SCA. In order to get access to private information, PA attacks take advantage of the link between the instantaneous current drawn from the device's power source and the data being processed or stored by the device. As the primary location for both program code and data storage, embedded memories are a crucial part of many cryptographic systems, including smart cards and wireless networks that make use of cryptography methods. Therefore, it is crucial to analyze and create safe memory. The 6T SRAM macrocell is widely used because of its high density, resilient operation, and great performance in embedded memory. The security features of 6T SRAM arrays are routinely neglected in favor of increasing their density and performance, making them very vulnerable to PA attacks. To mitigate the link between a standard 6T SRAM array's dynamic power dissipation and the information it stores, previous research have suggested redesigned SRAM bitcells [14, 15].

These two options both involve a two-step writing process. To prevent the write operation from being affected by the data already stored in the SRAM cell, the internal nodes (Q and QB) are pre-charged to a constant voltage in the first stage. Rather of utilizing the original 6T SRAM's power supply for the extra pre-charge phase, the authors of recommended employing two extra PMOS transistors to complete the task. In order to prevent shortcircuit power dissipation, the authors developed a feedback-cut SRAM cell, which consists of two extra NMOS transistors. These approaches significantly lessen the link between the SRAM array's power consumption and the information it stores, but at the expense of substantial delay, more power consumption, and lower static noise margins (SNMs). In this study, we detail a unique security-oriented 7T SRAM cell design that uses a two-phased write operation to drastically lower the correlation between the memory's power dissipation and the data being written or stored there, resulting in a memory that is resistant to PA attacks.

To ensure that the Q and QB voltages are equalized during the initial phase of the write operation, the proposed 7T cell adds an extra transistor to the original 6T SRAM design and a single power gate transistor per memory word. Security systems are increasingly at risk from power analysis (PA) assaults, which may reveal sensitive information by analyzing the current drawn from the system's power source. Many of these systems rely heavily on embedded memories, which are often

implemented using static random access memory (SRAM) cells with six transistors (6T). However, because to the close relationship between the properties of the current flowing through a standard SRAM cell and the data stored in it, these cells are vulnerable to attacks based on side-channel power analysis. We propose a security-focused 7T SRAM cell that adds a transistor to the standard 6T SRAM implementation and features a two-phase write operation to provide resistance to such attacks by drastically decreasing the correlation between stored data and power consumption during write operations.

We propose a modified 7T SRAM cell that uses a two-phase write operation consisting of an equalization and write phase to address the information leakage of the 6T SRAM cell during write operations, resulting in a significantly lower correlation between its current dissipation and the stored data in the cell. Fig. 2 is a diagrammatic depiction of the 7T SRAM cell that we propose. To prevent power loss due to a short circuit during the equalization phase of a write operation, a power gate PMOS transistor (PG) is utilized to turn off the voltage supply for an entire memory word (VVDD).

In order to reduce the length of Q and QB while equalizing, a transistor PPC is added to the original 6T SRAM design. By employing a PC signal to deactivate PG and enable PPC, the voltage between Q and QB may be equalized by charge-sharing without drawing any more power from the source. PC is drained during the second phase of the write operation to charge VVDD and turn off PPC, and then charged to turn on the NMOS access transistors (NA1 and NA2), which transmit the data from BL and BLB to Q and QB, respectively.

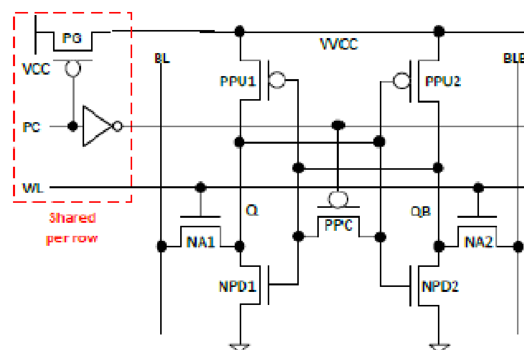

Fig. 1: 7T SRAM cell

PROPOSED METHOD

In recent years, low power IC design has been a focus due to the proliferation of portable battery-operated gadgets. These days, system-on-chips (SoCs) can't function without embedded SRAM devices. Traditional SRAM cell designs are inefficient and power-hungry in today's age of rapid mobile computing. Leakage currents account for the vast majority of the power needed to run integrated circuits, especially as technology speeds up and their sizes become smaller. In high-performance microprocessors and systems-on-a-chip (SoCs), leakage currents are mostly generated by memory banks. Leakage power consumption by memory arrays grows with each new generation of technology because more and more SRAM cells must be packed into integrated circuits to fulfill the demanding performance requirements. The reliability of stored information is another major issue with SRAM chips. Maintaining data stability in SRAM design has become more difficult due to decreases in supply voltage, smaller devices, and more severe process fluctuations. Therefore, there is a great need for innovative memory circuits that improve both leakage and data stability. Since memories are included in almost all modern electronic devices, cutting down on their power consumption and footprint is crucial for enhancing system performance, efficiency, and dependability. SRAM cells are widely used in embedded and portable systems because to their convenience and minimal standby leakage. Two inverters connected in a cross-coupled fashion are included in the innovative SRAM cell suggested here. A 7T SRAM with two pull-up and two pull-down transistors, two PMOS pass transistors, and one NMOS footer transistor is presented. Since NMOS devices have a higher leakage current compared to PMOS devices of the same feature size. The pass transistors of

SRAM cells are changed from NMOS to PMOS, and the leakage path from supply to ground is shortened by employing the footer nmos transistor. Since leakage power is a big issue with older technology, it is important to find ways to minimize it.In addition, we used a transistor with sl input.

In SRam, we perform:

Process of reading:

In order to conduct a read operation, memory must first contain data. So, let's assume Q=1 and Q'=0 in memory. In order to read, the word line must be brought up high. Since bits and bits_b are used as output lines, they are originally precharged to a node voltage of Vdd. Since Q and bit are large, the circuit will not discharge. Bit_b's voltage drops because there is a voltage disparity between Q' and the node voltage there and Q' is zero. As a result, the circuit will discharge, allowing current to flow.

The sense amplifier is a comparator that receives inputs from bit and bit_b; when bit' is low, the output is 1. Since Q was set to 1, the result was 1, validating the read operation. Similarly, think of Q in memory as equal to 0 and Q' as equal to 1. Since there is a voltage differential in the circuit, a discharge will occur at Q and bit. The transistors need a ratio where Q is less than P2/D2's threshold. Reading limits are what we refer to here. The output will always be 0 if the bit voltage is less than 1.When Q is set to 0, the result is also 0. As a result, read validity is confirmed in both instances.

Performing a Writ:

Assume Q=0 and Q'=1 make up the memory bits. Since the word line was high to begin with, a write operation could be executed. For the write operation, the input lines are bit and bit'. In order to measure the voltage difference between Q' and bit_b, we must first connect bit_b to ground, as we control the bit lines. Changing the transistors' aspect ratio makes D2 more powerful than P2, which is required for writing 1 into the SRAM cell. Therefore, Q equals 1. Since Q=0 before the operation and Q=1 afterwards, our memory write succeeds.

Put on the Brakes:

Turning off wordline in retention mode also turns off two pass gates. The cross-coupled inverters then create a feedback loop, so information is preserved while the power is on Model of the Proposed SRAM

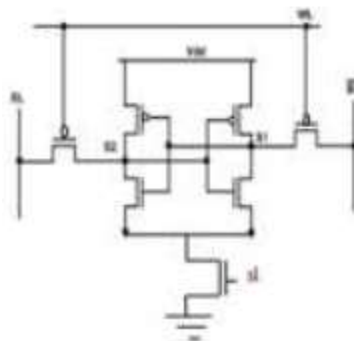

Fig. 2 Proposed SRAM

RESULTS:

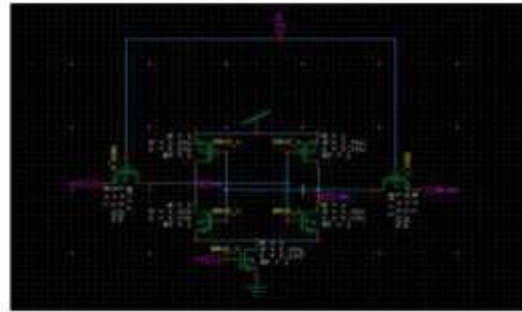

Fig. 3: Schematic of Proposed SRAM

Execution of a Write-1: Data is written to an SRAM cell through its bit line BL during the write operation mode. The BLB and WL lines are used during the writing process. After a "1" is entered into the cell, the BL is connected to VDD, the WL signal is enabled by M5, the "Q" node begins charging, and the "QB" node is flipped to logic "0" by M4's leads. Then, the 'QB' node facilitates the M1's ability to write logic 1'at the 'Q' node. If the data to be written is a '0,' then the WL signal is enabled and M5 goes on. This is the write-0 operation. Finally, the logic '1' is set at the node 'QB' when the node 'Q' begins discharging and activating M3. Next, 'QB' aids in activating M2, which enables appropriate discharging of the 'Q' node, yielding a '0' in logic at the 'Q' node. Counting by ones and zeros: The data stored in an SRAM cell is retrieved during the Read process. At the outset, the bit line data is pre-charged to VDD. The read signal is initiated when the bit line has been pre-charged. Whether information stored in RBL is retained or erased is determined by a single SRAM cell. When the read line is pulled to VDD, the RBL is discharged, and the SRAM cell is seen to have a "0" value. If it can maintain the charge, then it will record a 1. If the logic level of the read operation, WL, is 0, the read operation is disabled.

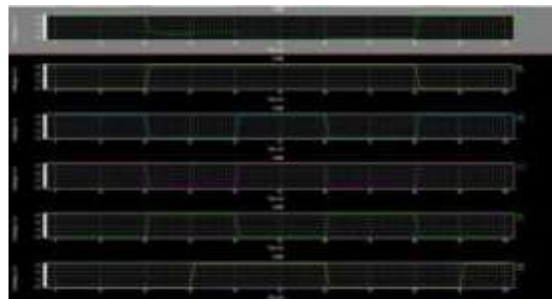

Fig.4:Waveform of Proposed SRAM

Timetable slip:

Fig.5:Area of Proposed SRAM

As technology levels drop, the margin for static noise becomes less. The Static Noise Margin is equal to the longest side of the square that fits exactly within the butterfly curve. As technology nodes decrease, SRAM's read and write stability properties are in risk of degrading. 7T SRAM can outperform 6T at low VDD, but it has severe limitations.

factors:

This 7T SRAM is limited in its low-voltage performance by the size of its transistors; the following diagram compares its performance up to the values of VDD = 0.72v and VSS= 0.36v. Since the write margin decreases with decreasing VDD, operating 7T SRAM below the specified voltage levels renders the write operation impossible. The leakage current of PMOS transistor P2 causes storage data annihilation in SRAM cells when a read operation is performed at low-VDD-: Levels. The figures illustrate this point when the 6T SRAM cell is used in a low-voltage mode. Proposed SRAM Delay

Fig.5: Delay of Proposed SRAM

Vital information:

Multiplying the average current taken from the source by the voltage given by the source yields the total power used by the source.According to the ITRS roadmap for 32 nm technology, the simulation use a power supply voltage of 0.9 V. Since the static power is exponentially proportional to the threshold voltage, an increase in the diameter variation results in a corresponding increase in the static power required to maintain a constant voltage across the circuit. When compared to a standard 6T SRAM cell, the proposed 7T SRAM uses 22.03% less power during a write '0' operation, 17.33% less power during a write '1' operation, 17.52% less power during a read '0' operation, and 21.36% less power during a read '1'

Fig.7: Power of Proposed SRAM

Conclusion:

A 7T SRAM architecture was described in this work. To lower the static circuit power consumption, the suggested SRAM employs a footer nmos switch with input sl. The suggested sram cell is created in tanner utilizing 90nm technology. Our simulation findings demonstrate that the suggested circuit improves upon the state-of-the-art in terms of energy dissipation.

Prospective Range:

There is potential for future studies to include the suggested DFF into complicated digital systems that use a mixture of sequential and combinatorial logic. Integrating the suggested DFF into complicated digital systems that use sequential and combinatorial logic is a possible direction for future study. Integrating the suggested DFF into complicated digital systems that use sequential and combinatorial logic is a possible direction for future study. Future iterations of power-hungry applications, such as EMBEDED SYSTEMS and central processing units (CPUs), will be able to make use of the

suggested SRAM. Not only is this sram cell great for all sorts of portable applications, but integrating it into an array reduces the array's total power consumption. Integration of the suggested DFF into complex digital systems that make use of both sequential and combinatorial logic is a potential area for further investigation.

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